Notice of Allowability	Application No. 10/625,945	Applicant(s) JEX ET AL.	
	Examiner YOUNG T. TSE	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 30 June 2007*.

2. ☒ The allowed claim(s) is/are *1-11,13-20 and 22-28*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____ .
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____ .

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In claim 1, line 8, "have" has been changed to "has".

In claim 10, line 9, "have" has been changed to "has".

In claim 23, line 8, "the full cycle" has been changed to "the cycle".

In claim 27, line 2, "the full cycle" has been changed to "the cycle".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YOUNG T. TSE
Primary Examiner
Art Unit 2611

Amendments to the Claims:

Please amend the claim as follows in a complete set of the claims.

Claims (complete set).

1. (Currently amended) A chip comprising:

a transmitter including a cycle encoding circuit to receive a data input signal and to provide a full cycle encoded signal in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals, and wherein data is represented in data time segments of the full cycle encoded signal and no data time segment has more than one cycle of an encoding signal;

wherein each of the data time segments ~~have~~ has the same time duration; and

wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal.

2. (Original) The chip of claim 1, wherein the transmitter further includes a complementary cycle encoding circuit to receive the data input signal and to provide a complementary full cycle encoded signal in response thereto.

3. (Currently amended) The chip of claim 1, wherein the multiplexer is to select the portions of the encoding signals that are to form the full cycle encoded signal in response to which encoding signal was selected for a previous data time segment.

4. (Original) The chip of claim 1, further comprising a periodic signal source to provide a periodic reference signal and wherein the transmitter includes circuits to provide the encoding signals in response to the periodic reference signal.

5. (Original) The chip of claim 4, wherein the periodic reference signal has period that is equal to the time length of the data time segments.

6. (Original) The chip of claim 4, wherein the periodic reference signal has a period that is equal to the time length of a data bit cell of the data input signal.

7. (Original) The chip of claim 1, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

8. (Original) The chip of claim 1, wherein the full cycle encoded signal represents a 0 or a 1 depending on the value of the data.

9. (Previously presented) The chip of claim 1, further comprising a receiver that includes an initial receiving circuit to receive the full cycle encoded signal, a delay circuit to delay at least one signal provided by the initial receiving circuit, and a logic circuit to receive at least one signal from the delay circuit and in response thereto to provide a data out signal which includes recovered data from the full cycle encoded signal.

10. (Currently amended) A chip comprising:

a transmitter including a cycle encoding circuit to receive a data input signal and a periodic reference signal and to provide a cycle encoded signal in response thereto, wherein in response to the data input signal and the periodic reference signal, the cycle encoded signal is formed of continuously joined portions of encoding signals during successive data time segments, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals;

wherein each of the data time segments ~~have~~ has the same time duration;

wherein the transmitter further includes a complementary cycle encoding circuit to receive the data input signal and the periodic reference signal and to provide a complementary cycle encoded signal in response thereto, wherein the complementary cycle encoded signal is a logical inverse of the cycle encoded signal; and

wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal.

11. (Original) The chip of claim 10, wherein the cycle encoded signal is a full cycle encoded signal in which no data time segment has more than one cycle of an encoding signal.

12. (Canceled)

13. (Original) The chip of claim 10, wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the cycle encoded signal in response to the data input signal and which encoding signal was selected for a previous data time segment.

signal and which encoding signal was selected for a previous data time segment.

19. (Original) The system of claim 16, further comprising a periodic signal source to provide a periodic reference signal and wherein the transmitter includes circuits to provide the encoding signals in response to the periodic reference signal.

20. (Original) The system of claim 16, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

21. (Canceled)

22. (Previously presented) The system of claim 16, wherein the recovered values are the inverse of those of the data input signal.

23. (Currently amended). A system comprising:

a transmitter including:

(a) a cycle encoding circuit to receive a data input signal and to provide a cycle encoded signal in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals, wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the ~~full~~ cycle encoded signal in response to the data input signal; and

(b) a complementary cycle encoding circuit to receive the data input signal and to provide a complementary cycle encoded signal in response thereto by continuously joining portions of the different encoding signals; and

a receiver to receive the cycle encoded signal and the complementary cycle encoded signal and to recover values of the data input signal in response thereto.

24. (Currently amended) The system of claim 23, wherein data is represented in data time segments of the cycle encoded signal and wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the cycle encoded signal in response to the data input signal and which encoding signal was selected for a previous data time segment.

25. (Original) The system of claim 23, further comprising a periodic signal source to

provide a periodic reference signal and wherein the transmitter includes circuits to provide the encoding signals in response to the periodic reference signal.

26. (Original) The system of claim 23, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

27. (Previously presented) The system of claim 23, wherein the receiver includes an initial receiving circuit to receive the ~~full~~ cycle encoded signal, a delay circuit to delay at least one signal provided by the initial receiving circuit, and a logic circuit to receive at least one signal from the delay circuit and in response thereto to provide a data out signal which includes the recovered values of the data input signal.

28. (Currently amended) The system of claim 23, wherein data is represented in data time segments of the cycle encoded signal and wherein the cycle encoded signal is a full cycle encoded signal in which no data time segment has more than one cycle of an encoding signal.